WHAT IS CLAIMED IS:

1. A semiconductor device comprising:

a semiconductor element having a circuit surface on which a plurality of circuit electrodes are disposed, said circuit surface being coated with a protecting film,

a stress relaxation layer which is formed on the protecting film of the circuit surface of said semiconductor element so as to expose the circuit electrodes, is made of a cured thermoplastic resin and has an inclination in the edge portion thereof,

a wiring layer consisting of a plurality of wirings, each of said wirings being connected to one of the circuit electrodes and disposed so as to make an electrical connection from said circuit electrode, via the edge portion of stress relaxation layer and to a desired site on the surface of the stress relaxation layer,

a surface protecting film which covers the surface of the wiring layer so as to expose a prescribed portion on each of the plurality of wirings on the surface of the stress relaxation layer, and

an external connection terminal formed by connecting a bump to said prescribed exposed portion of each of the plurality of wirings.

2. A semiconductor device according to Claim 1, wherein a swelling portion is formed in the surrounding part connected to the inclined edge portion of the

stress relaxation layer and a deflected portion is formed in the wiring existing on said swelling portion.

3. A semiconductor device according to Claim 1 or 2, wherein the melting temperature Tm of the cured thermoplastic resin in said stress relaxation layer is not lower than the maximum attainable temperature Tmax in the process of forming said wiring layer and surface protecting layer.

4. A semiconductor device according to Claim 1 or 2, wherein the melting temperature Tm of the cured thermoplastic resin in the stress relaxation layer is not lower than 350°C.

5. A semiconductor device according to Claim 1 or 2, wherein glass transition temperature Tg of the cured thermoplastic resin in said stress relaxation layer is in the range of from 150°C to 400°C.

6. A semiconductor device according to Claim 1 or 2, wherein coefficient of thermal expansion of the cured thermoplastic resin in said stress relaxation layer is not greater than 200 ppm/°C.

7. A semiconductor device according to Claim 1 or 2, wherein thickness of said stress relaxation layer is in the range of from about 35 μm to about 150 μm.

8. A semiconductor device according to Claim 1 or 2, wherein the cured thermoplastic resin in said stress relaxation layer is at least one member selected from the group consisting of polyimide, polyamide, polyamide-imide, epoxy, phenolic and silicone.

9. A semiconductor device according to Claim 1 or 2, wherein the protecting film formed on the semiconductor element is constituted of an inorganic film and an organic film locally formed on said inorganic film.

10. A semiconductor device according to Claim 1 or 2, wherein the wirings are formed so that the width of the wiring in the edge portion of said stress relaxation layer is greater than the width of wiring in the flat portion of said stress relaxation layer, at least regarding signal wirings.

11. A semiconductor device according to Claim 1 or 2, wherein said wiring layer is constituted of an electric power supply film layer contact-bonded to the surface of said stress relaxation layer and a plating film layer.

12. A semiconductor device comprising:

a semiconductor element having a plurality of circuit electrodes disposed thereon and a circuit surface coated with a protecting film,

a stress relaxation layer formed on the protecting film of the circuit surface of said semiconductor element so as to expose the circuit electrodes, which is made of a cured resin having a glass transition temperature Tg falling in the range of from 150°C to 400°C and has an inclination in the edge portion thereof,

a wiring layer consisting of a plurality of

wirings, each of said wirings being connected to one of the circuit electrodes and disposed so as to make en electrical connection from said circuit electrode, via the edge portion of stress relaxation layer and to a desired site on the surface of the stress relaxation layer,

a surface protecting film which covers the surface of the wiring layer so as to expose a prescribed portion on each of the plurality of wirings on the surface of the stress relaxation layer, and

an external connection terminal formed by connecting a bump to said prescribed exposed portion of each of the plurality of exposed wirings.

13. A semiconductor device according to Claim 12, wherein thickness of said stress relaxation layer is in the range of from about 35 μm to about 150 μm.

14. A mounted structure of semiconductor device constituted by mounting a semiconductor according to any one of Claims 1 to 13 on a circuit substrate by connecting an external connection terminal of said semiconductor device to an electrode formed on said circuit substrate.

15. A process for manufacturing a semiconductor device which comprises

a wafer-producing step for producing a wafer having a plurality of semiconductor elements disposed thereon having a circuit surface on which a plurality of circuit electrodes are disposed,

a protecting film-forming step for forming a protecting film on the circuit surface of each semiconductor element, which is in the state of a wafer produced in said wafer-producing step,

a stress relaxation layer-forming step which comprises forming a stress relaxation layer having an inclination in the edge portion thereof on the protecting layer by printing a thermoplastic resin paste onto the protecting film of wafer state formed in said protecting film-forming step by the mask printing method so as to expose said circuit electrodes, followed by curing the printed stress relaxation layer,

a wiring layer-forming step for forming a wiring layer consisting of a plurality of wirings, each of said wirings being connected to one of the circuit electrodes in the above-mentioned wafer state and disposed so as to make an electrical connection from the circuit electrode, via the edge portion of the stress relaxation layer formed in the stress relaxation layer-forming step, to a desired site on the surface of the stress relaxation layer,

a surface protecting film-forming layer for coating the surface of the wiring layer of wafer state formed in the wiring layer-forming step with a surface protecting film so as to expose a prescribed portion of the plurality of wirings on said stress relaxation layer,

an external connection terminal-forming step

for connecting a bump to each prescribed portion of the plurality of wirings exposed in the wafer state, and

a dicing step for dicing the wafer state of product into a desired unit to obtain a semiconductor device.

16. A process according to Claim 15, wherein said wiring layer-forming step comprises a sputtered film-forming step and a plated film-forming step.